REMARKS

Claims 1-26 and 29-35 are all the claims pending in the application. Claims 8-15 and 22-26 have been withdrawn from consideration. Claims 1-7, 16-21, and 29-32 stand rejected. Claims 33-25 are hereby newly added. Support for claims 33-35 can clearly be found throughout the Applicant's Specification.

Claims Rejection - 35 U.S.C. § 102

Claims 1, 3, 6-7, 29 are rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Akiyama et al. (J.P 11-194316, hereinafter "Akiyama"). For at least the following reasons Applicant traverse the rejection.

Independent claim 1

Akiyama does not disclose all the features of the claimed invention. Claim 1 recites *inter alia,* at least one capacitance load connected to respective terminals of said first and said second transistors not connected to said first and second voltage supplies. However, Transistor TR3 cannot be the at least one first transistor and transistor TR4 cannot be the second transistor, as the Examiner alleges. *See* Office Action, pg. 5. In Fig. 6 of Akiyama, the capacitor C1 and VDD are both connected directly or indirectly to the source terminal of TR3. Similarly, TR4's source terminal is connected to both C2 and VEE. Therefore, the capacitance and the voltage supplies in Akiyama are both connected to the same terminal of the transistors TR1 and TR2, unlike the claimed invention, which requires that they be connected to different terminals.

Furthermore, the Examiner alleges that transistors TR1 and TR2 also serve as the alleged first and second transistors. However, Applicant respectfully disagrees and asserts that Akiyama

does not disclose at least one signal line connected to each gate terminal of said first and second transistor. VCOM alleged to be the at least one signal line is connected to the drains of transistors TR3 and TR4. *See* Fig. 6.

Furthermore, there is no disclosure of a high level of signal passing through the at least one signal line is higher than the high level voltage signal supplied by the first voltage supply and a low level signal passing through the signal line is lower that the low level voltage signal supplied by the second voltage supply, as recited in claim 1. The Examiner merely points to VDD, VEE and section 47. However, as illustrated in Fig. 6 of Akiyama, a multiplexer is driven by +VDD and -VEE. Therefore, the upper limit level of the signal output from the multiplexer can be expected to be +VDD and the lower limit level to be -VEE. Accordingly, Applicant respectfully requests the withdrawal of the rejection of claim 1 because Akiyama does not disclose all the features of the claimed invention.

Dependent Claims 3, 6-7, 29

Dependent claims 3, 6-7, 29 are believed to be allowable at least by virtue of their dependency on independent claim 1.

Furthermore, with respect to claim 3, as discussed above VCOM is connected to the drains and not the respective gates of the transistors. Accordingly, claim 3 is allowable for this additional reason.

Furthermore, with respect to claim 6, Akiyama, para. 12 merely discloses that a transistor which composes pixels is TFT 24. However, Akiyama fails to disclose that the transistor

provided in VCOM driver circuit is TFT. Accordingly, claim 6 is allowable for this additional reason.

Furthermore, with respect to claim 29, Akiyama does not disclose a level shift circuit connected to said one signal line directly or via a buffer circuit. Para. 14 of Akiyama merely discloses that driver 12 includes D/A conversion circuit which converts gradation data into the voltage of the signal. Accordingly, claim 29 is allowable for this additional reason because Akiyama does not disclose a level shift circuit as recited in the claimed invention.

Claim Rejections - 35 U.S.C. § 103

Claims 2, 16-21, 30-32 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Akiyama in view of Hosokawa et al. (US Patent No: 4,393,380, hereinafter "Hosokawa").

Claims 4-5 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Akiyama in view of Taki (U.S. 2002/000833, hereinafter "Taki")

Claims 19-20, 32, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Akiyama in view of Hosokawa and Taki.

Applicant respectfully traverses these rejections.

Claims 2 and 16

Hosokawa fails to make up for the deficiencies of Akiyama with respect to claim 1. Therefore, claim 2 is believed to be allowable at least by virtue of its dependency on independent claim 1.

Furthermore, with respect to claim 2 and 16, the Examiner correctly admits that Akiyama fails to disclose the limitation "wherein the common drive circuit is disposed on a position opposite to the gate driver circuit and the display portion therebetween" recited in claim 2 and 16. *See* Office Action page 3. The Examiner cites Hosokawa to make up for this deficiency of Akiyama. The Examiner states that Hosokawa discloses capacitor common drive circuit 34 (alleged common drive circuit) and row electrode drive 2 (alleged gate driver) opposite to each other with the display therebetween. See Office Action pg. 4 and Fig. 4 of Hosokawa.

The Examiner further states that it would have been obvious to have the common drive circuit be positioned to the gate driver circuit with the display portion in between as taught by Hosokawa with the common drive circuit of Akiyama, since the repositioning of these elements is in no way critically dependent upon the overall operation of the display, and further this configuration could be combined to achieve the predictable result of space and cost efficiency when a display is located in a compact area. *See* Office Action, pg. 6.

Applicant respectfully submits that one skilled in the art would not modify or rearrange the components of Akiyama because there is no reason or rationale in the prior art for making such a modification. The Examiner loosely states because there is no critical dependency from the reposition of the elements, it would be obvious to combine them, but the standard for obviousness is not the lack of critical dependency rather the Examiner must offer some form of explicit motivation to combine the two references. Applicant also submits that the Examiner's reason for modifying Kumada does not establish a *prima facie* case of obviousness because the

Examiner does not indicate how cost and space efficiency occurs when a display is located between a gate driver and a common drive circuit. Therefore, claims 2 and 16 are allowable.

Dependent claims 4, 5 and 30

Taki fails to make up for the deficiencies of Akiyama with respect to features of claim 1. Accordingly, claims 4, 5 and 30 are believed to be allowable at least by virtue of their dependency on independent claim 1.

Furthermore, claim 30 is patentable at least for reasons discussed above with respect to claim 29.

Dependent Claim 17

Claim 17 is patentable at least for reasons discussed above with respect to claim 1. Claim 17 is also patentable at least by virtue of its dependency.

Dependent Claims 18-21 and 31-32

Taki and Hosakawa fail to make up for the deficiencies of Akiyama. Therefore, claims 18-21 and 31-32 are believed to be allowable at least by virtue of their dependency on claim 17.

Furthermore, claim 18 is patentable at least for reasons discussed above with respect to claim 3.

Furthermore, claim 19 is patentable at least for reasons discussed above with respect to claim 4.

Furthermore, claim 20 is patentable at least for reasons discussed above with respect to claim 5.

Furthermore, claim 21 is patentable at least for reasons discussed above with respect to claim 6.

Furthermore, claim 31 and 32 are patentable at least for reasons discussed above with respect to claim 29.

Claim Additions

The Applicant has added claims 33-35. Support for these claims can clearly be found throughout the Applicant's Specification. Claims 33 and 34 contain features that are similar to features of claim 1. Therefore, they are believed to be allowable for analogous reasons. Claim 35 is believed to be allowable at least by virtue of its dependency on independent claim 1.

Furthermore, with respect to claim 33, in an exemplary embodiment of the present invention, since TFT which configures active matrix is added high voltage in general, the TFT has a characteristic for enduring with high voltage. The characteristic is applied to the first and the second transistors of the exemplary embodiment of the present invention. Therefore, a high amplitude signal can be added to the first and the second transistors of which high level is higher than the voltage of the first power supply and of which the low level is lower than the voltage of the second power supply. Accordingly, on-resistance of transistors can be reduced. *See* Applicant's Specification, para. 41. Thereby, high voltage power supply provided in a gate driver can be used as the first and the second power supply. Accordingly, claim 33 is allowable for this additional reason.

Furthermore, with respect to claim 34, Akiyama does not disclose that a source or drain of the first transistor connects directly with the first power supply and a drain or source of the second transistor connects directly with the second power supply. Accordingly, claim 34 is allowable for this additional reason.

Furthermore, with respect to claim 35, Akiyama fails to disclose that the at least one capacitance is directly connected to respective terminals of said first and second transistors. Accordingly, claim 35 is allowable for this additional reason.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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